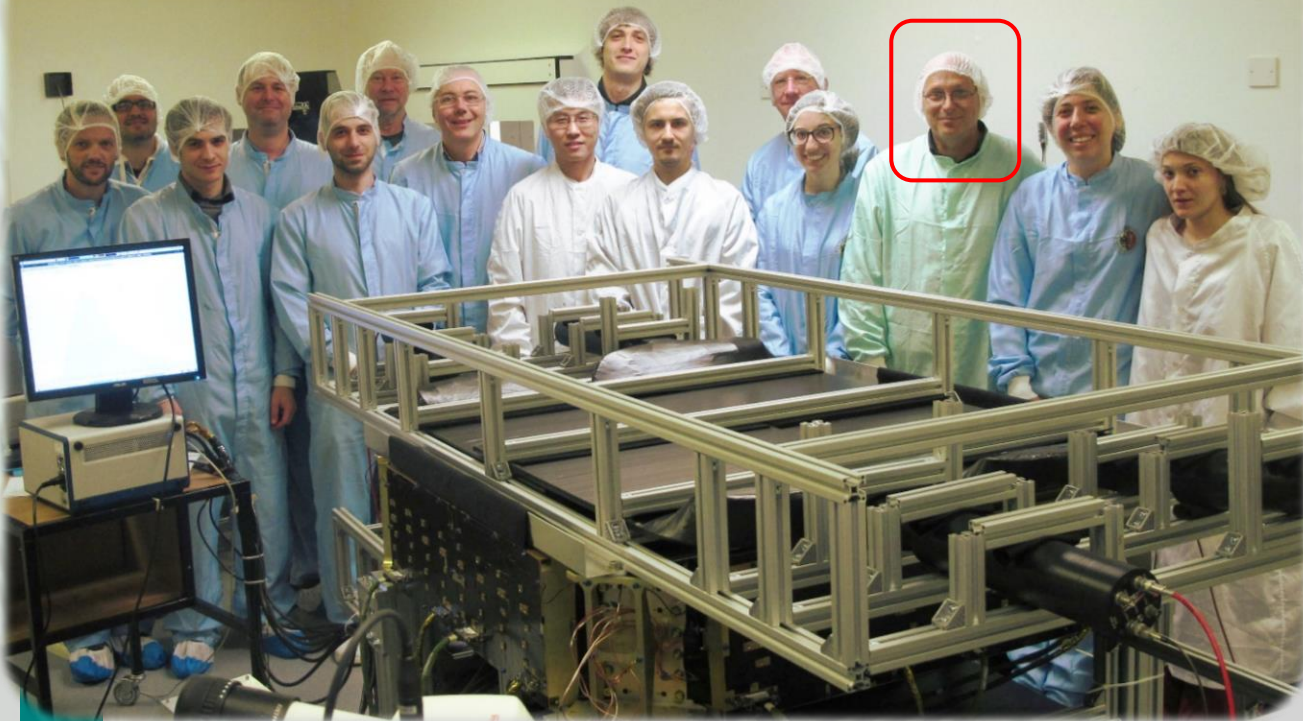




Retraite Daniel La Marra

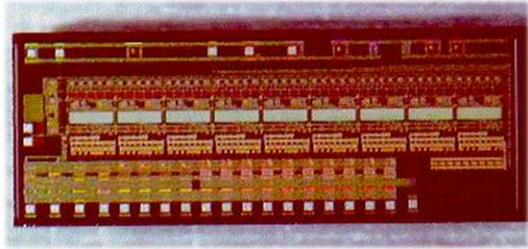
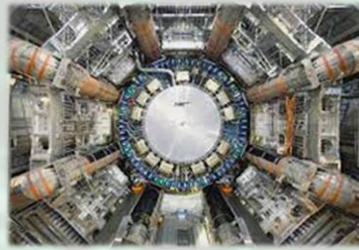
1980 - 2021 (?)

DAMPE space experiment



GVA red wine
'space' experiment

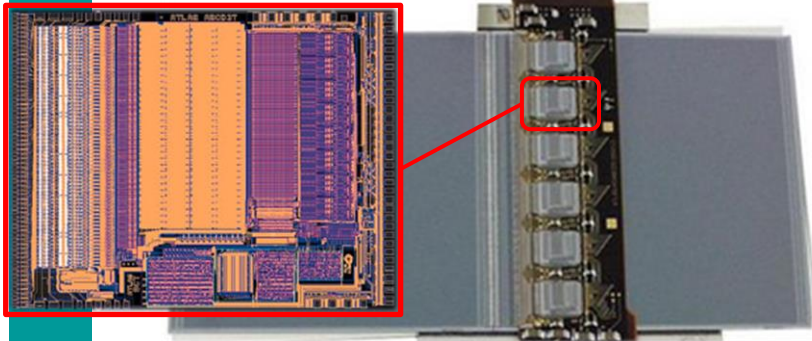




CRIAD ADC chip

Microelectronics Digital design

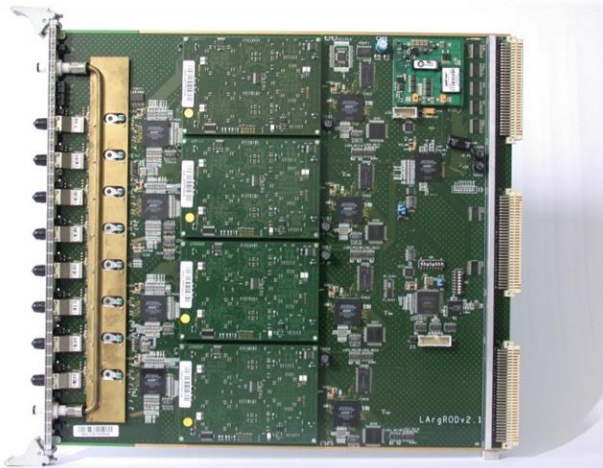
1993 – CERN RD2/AMS detector



ABCD Chip

Microelectronics Digital design

1997 – CERN ATLAS Tracker Strips



LargROD back-end

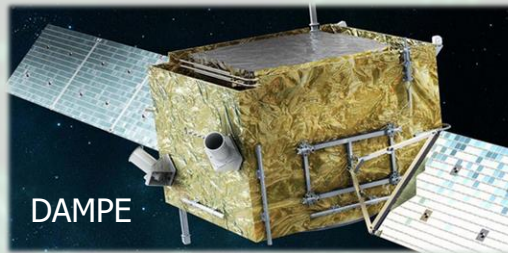
VME 9U optics PCB & FPGA design

250 Boards production

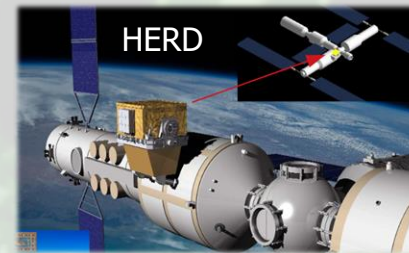
2009 – CERN ATLAS Liquid Argon



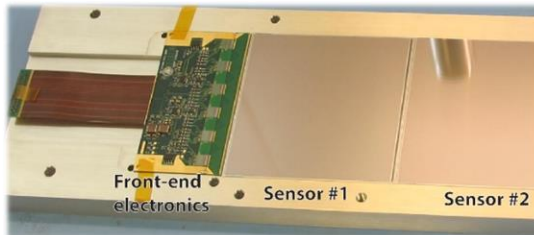
POLAR



DAMPE



HERD

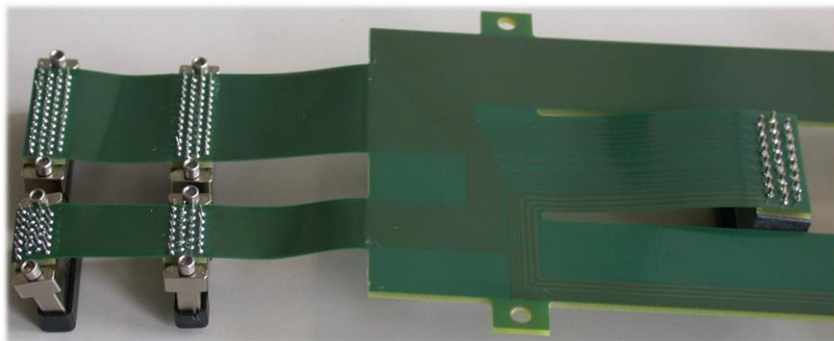


DAMPE STK Front-end

384-ch ASIC Flex-Rigid PCB design

200 Boards production

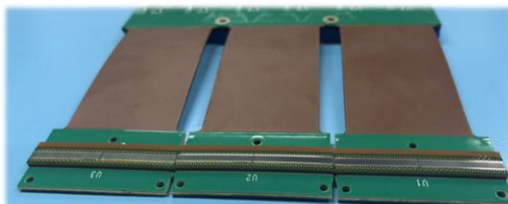
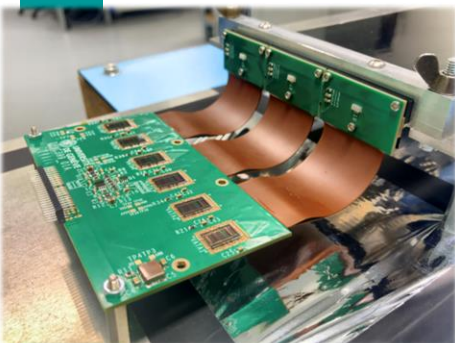
2015 – Chinese Satellite



POLAR Flex

Flex-Rigid PCB Design

2016 – Chinese Spacelab TG2



HERD R&D

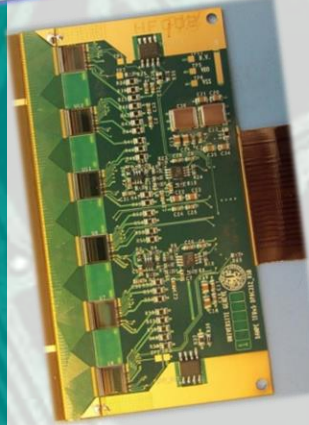
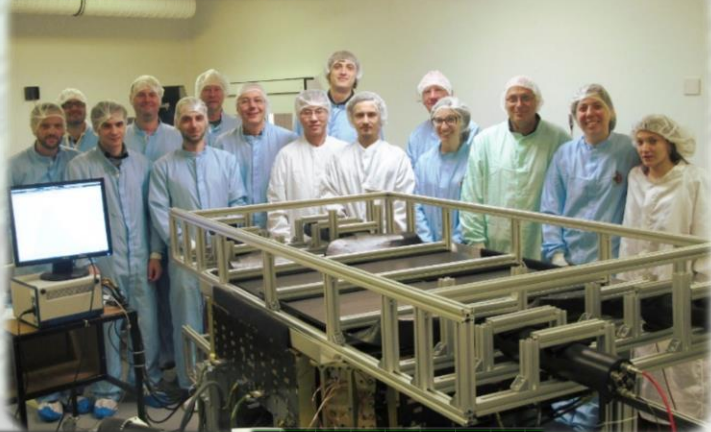
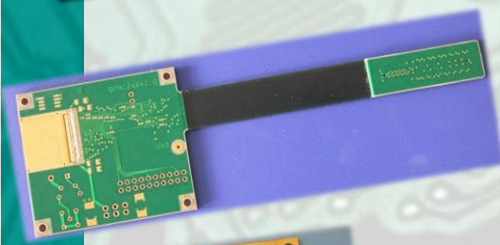
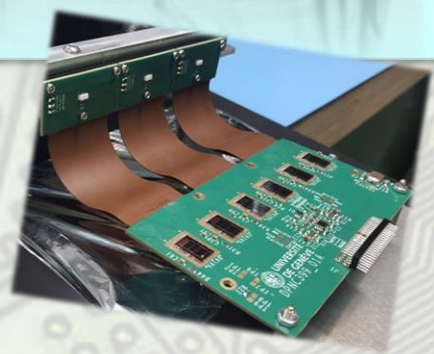
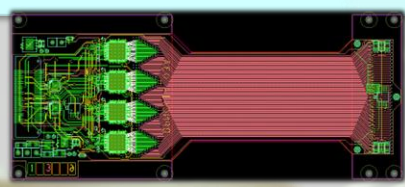
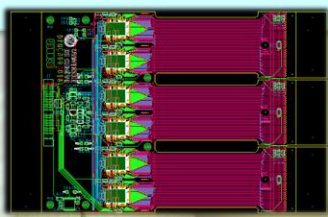
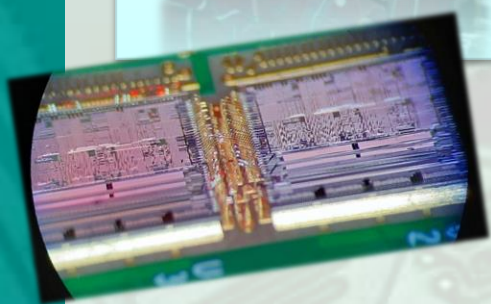
128-ch ASIC Flex-Rigid PCB design

~10 Prototypes

202x – Future Chinese Spacelab



Bonne Retraite Daniel !



```
-- FIFO TX will process
p_fifo_wr : process(all)
begin
  -- latched default values
  s1_next_counter <= s1_int_counter;
  s1_next_din <= s1_int_din;
  s1_next_wr <= '0';
  s1_next_state <= s1_int_state;
  s1_next_din(2) <= '0'; -- no packend end
  -- Intermediate
  s1_int_counter_compare <= s1_int_dpar_latch(C_LATCH_DPAR_LED3_BIT);

  case s1_int_state is
    when IDLE =>
      -- start request
      s1_next_din(s1 downto 0) <= X"00000000";
      if((s1_int_param_out(LEP_DECODER_ARG_READOUT_STOP_BIT)='0') and
        s1_next_state <= WRITING;
      s1_next_counter <= (others => '0');
      end if;
    when WRITING =>
      if (s1_int_DATA_FIFO_wrusdhw < C_FIFO_ALMOST_FULL) and (s1_int
        -- continuous write at main clock freq. when Leds value
        -- also partial write at main clock freq./led value > 0
```

